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Code No: B7704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012
CPLD & FPGA ARCHITECTURE AND APPLICATIONS
(EMBEDDED SYSTEMS & VLSI DESIGN)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks

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1.a) Compare PLA,PAL and PLD s with respect to different features, programming and applications.
b) Give the functional description of the Altera's MAX 7000 PLD with the help of logical array block and Macro cell Diagrams.

2.a) Explain how Actel's ACT2 FPGA Family is architecturally close to MPGA with neat diagram.
b) Explain how an FPGA can be chosen with different stages of Elimination trials and comparative evaluation.

3.a) Explain about the state assignment for FPGA
b) Give the basic properties of petrinet Explain the traffic light controller design using petrinet notation.

4.a) Design a one to three pulse generation by using a PLA to generate the next state and output.
b) Explain the application of the one Hot method to a serial 2's complement.

5.a) Explain one of the Mentor Graphic's FPGA advantage tool feature of state machine Design Entry.
b) Explain the FPGA design flow with each level in the design.

6.a) Explain the extended petrinets for parallel controllers
b) Explain the datapath and functional partition of FSM system level design

7.a) Write the HDL code for the design of 4-bit parallel adder using four 1-bit parallel adders
b) Develop one hot state diagram for a sequence checker whose output is '1' whenever the sequence 0101 is detected. Also specify the Transition Table.

8. Write short notes on any **Two**
a) State machine designs centered around shift registers
b) Realization of State machine chart using PAL
c) Technology mapping for FPGAs

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